B. Tech. (ECE) (Elective-II) 6th Semester
(G Scheme) Examination, July-2022

VHDL & DIGITAL DESIGN

Paper-PEC-ECE-312-G

Time allowed : 3 hours] *[Maximum marks : 75*

Note : *Attempt **five** questions in all, selecting at least **one** question from each section. **Question No. 1 is compulsory.** All questions carry equal marks.*

1. Define the following : 6×2.5=15

(a) Advantages of Computer aided designing.

(b) Categories of Delays in VHDL.

(c) Identifiers and extended Identifiers.

(d) Libraries in VHDL.

(e) Justify all the types of overloading with example.

(f) Entity and interface declaration.

Section-A

2. Discuss the three basic models for architecture declaration with suitable example. 15

or

3. Discuss all the types of operators used in VHDL and mention their declaration syntax. 15

Section-B

4. Compare between concurrent and sequential statement. Discuss all the categories of concurrent statement. 15

or

5. (a) Write short note on conditional statements used in VHDL. 7

   (b) Write short note on resolution function and generics. 8

Section-C

6. Develop the VHDL code for structural model of an encoder. 15

or

7. (a) Write the VHDL code for behavioural model of 4×1 multiplexer. 8

   (b) Write the VHDL code for dataflow model of a comparator. 7

Section-D

8. Differentiate between PAL and PLA. Discuss the designing of PLA in detail. 15

or

9. Draw and discuss the architecture of simple microcomputer structure. 15