# B. Tech. (ECE) 6th Semester (G Scheme) Examination, July-2022

## CMOS DESIGN

## Paper-PCC-ECE-308-G

*Time allowed : 3 hours]* *[Maximum marks : 75*

***Note :*** ***Question No. 1 is compulsory.*** *Attempt any* ***one*** *question each from* **Unit-I** *to* **Unit-IV.**

1. (a) What is channel length modulation ?

   (b) Write CMOS design rules.

   (c) Explain any 2 impacts of inter connect modeling.

   (d) Write note on timing matrices of sequential circuits.

   (e) What is gate leakage ? 5×3=15

### Unit-I

2. Explain working of n-type enhancement type MOSFET with its modes and regions. Draw characteristic curve also. 15

3. Explain R-C delay model. Draw circuit for R-C delay model for inverter and determine propagation delay. 15

## Unit-II

4. Explain static CMOS. Explain design techniques to reduce delay in it. 15

5. Explain interconnect modeling for resistance and inductance. 15

## Unit-III

6. (a) Explain block diagram of finite state machine using positive edge triggered registers. 10

   (b) Give differences between latch and registers. 5

7. (a) Explain Schmitt trigger with its CMOS implementation. 10

   (b) Give basics of synchronous timing design. 5

## Unit-IV

8. Explain architecture of 512–word content addressable memory. 15

9. What are address decoders ? Explain static decoder design. 15