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B.Tech. (ECE) 4th Semester (G-Scheme)  
Examination, July-2022  
DIGITAL ELECTRONICS  
Paper- PCC-ECE-205-G

Time allowed : 3 hours]

[Maximum marks : 75

*Note : Question no. 1 is compulsory. Attempt one questions from each unit.*

1. (a) What are the differences between Combinational Circuits and Sequential Circuits? 2.5
- (b) What are the applications of Demultiplexer? 2.5
- (c) What is the difference between Synchronous and Asynchronous Counters? 2.5
- (d) What are the applications of Flip-Flops? 2.5
- (e) What is Half-Adder? 2.5
- (f) What are the limitations of the Karnaugh Map? 2.5

**Unit - I**

2. Find a minimal SOP representation for  $f(A,B,C,D,E) = \sum m(1,4,6,10,20,22,24,26) + d(0,11,16,27)$  using K-map method. Draw the circuit of the minimal expression using only NAND. 15

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3. (a) List out the basic rules (laws) that are used in Boolean algebra expressions with example. 8
- (b) Implement the expression  $Y(A, B, C) = \Pi M(0, 2, 4, 5, 6, 7)$  using only NOR-NOR logic. 7

Unit - II

4. (a) Draw the block schematic of Magnitude comparator and explain its operation. 8
- (b) Draw & explain the block diagram of a 4-bit parallel Adder/Subtractor. 7
5. (a) Design & explain the working of Gray to BCD converter. 8
- (b) Explain even parity checker and generator. 7

Unit - III

6. (a) Design and explain the working of an 4-bit Parallel counter. 8
- (b) Design and explain the working of a BCD ripple counter with timing diagram. 7
7. (a) Explain the operation of universal shift register with neat block diagram. 8
- (b) Explain the working of Master/Slave JK FF. 7

Unit - IV

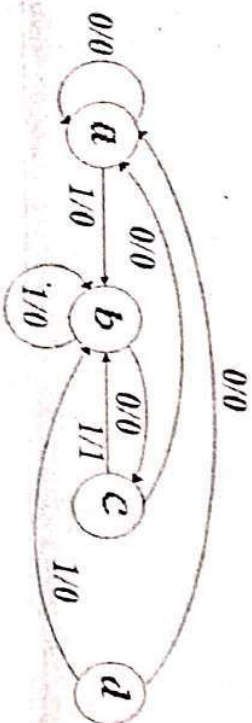
8. (a) Write a note on FPGA with neat diagram. 8
- (b) Write short notes on PLD, types of PLDs. 7

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9. Design a clocked sequential machine using JK flip flops for the state diagram shown in figure. Use state reduction if possible and make proper state assignment. 15



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