Roll No. : .....

Total No. of Questions : **9**] [Total No. of Pages : **3**

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B.Tech. (ECE) 6th Semester (Supplementary) Examination, July-2021

(G Scheme) (Elective-II)

VHDL AND DIGITAL DESIGN

Paper-PEC-ECE-312-G

*Time : **Three** Hours]* *[Maximum Marks : **75***

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note :- Question No. **1** is compulsory. Attempt *one* question from each Unit-I to Unit-IV.

1. (a) Write capabilities of VHDL.

   (b) Write a note on Libraries.

   (c) Write a program for half subtractor using data flow style of modeling.

(d) Write a note on process statement.

(e) Write a program for 4 : 2 encoder using case statement. 3×5=15

Unit–I

2. (a) Explain with examples data classes in VHDL.

(b) Explain types of operators in VHDL. 7,8

3. (a) Explain scalar types in VHDL.

(b) Explain types of delays in VHDL. 8,7

Unit–II

4. Explain functions with an example. Give differences between function and procedures. 15

5. (a) Write a program for 5-bit parity generator using structural style of modeling.

(b) Explain packages in VHDL. 10,5

Unit–III

6. (a) Write a program for full adder using behavioral style of modeling.

(b) Write a program for 4-bit comparator using If statement. 8,7

7. (a) Write a program for 4 : 1 multiplexer using case statement.

(b) Write a program for 3-bit parallel in parallel out shift register. 10,5

Unit–IV

8. Explain PLA with block diagram. 15

9. Write notes on the following :

(a) ROM

(b) FPGA 7½×2=15