

Roll No. :

Total No. of Questions : 9]

[Total No. of Pages : 3

3326

**B.Tech. (ECE) 6th Semester (Supplementary)
Examination, July-2021
(G Scheme)**

CMOS DESIGN

Paper-PCC-ECE-308-G

Time : Three Hours]

[Maximum Marks : 75

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note :- Question No. 1 is compulsory. Attempt one question each from Unit-I to Unit-IV.

1. (a) What are mobility degradation and velocity saturation ?
- (b) Write the various design rules for CMOS.
- (c) Draw circuit for CMOS inverter and explain its working.

(d) What is power gating ?

Unit-IV

15 each

(e) Explain pseudo-nMOS circuit.

3×5=15

Unit-I

15 each

2. Derive equation for drain current for MOSFET. Draw characteristic curve.

3. Explain the various types of capacitance in MOSFET. Draw C-V characteristics.

Unit-II

15 each

4. Explain static CMOS power sources.

5. Explain the various impacts of interconnect modeling.

Unit-III

15 each

6. (a) Explain timing metrics of sequential circuits.

(b) Give differences between latch and registers.

(c) Explain bistability principle.

7. Explain the timing classification of digital systems.

8. Explain array structured memory organization.

9. Explain column and block decoders.

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