5E3253-R

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B. Tech. (Sem. V) (Main) Examination, December - 2011
5CS2 Digital Logic Design

Time : 3 Hours] [Maximum Marks : 80
[Min. Passing Marks : 24

Instructions to Candidates :

*Attempt any **five questions** selecting **one question** from **each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.*

Use of following supporting material is permitted during examination.
(Mentioned in form No. 205)

1. NIL 2. NIL

UNIT - I

1 (a) Why we use hardware description language and explain what is use in digital logic design ? 8

(b) Explain different data type in HDL modeling. 8

OR

1 (a) Explain different type of modeling in VHDL with example. 8

(b) Write a program of Ripple Carry adder in VHDL language. 8

UNIT - II

2 (a) Explain different kinds of subprogram with examples. 8

(b) Write a behavioural description of a D-flipflop. 8

OR

2 (a) What is difference of Generate and concurrent statement ? Explain with suitable example.

8

(b) What is simulation and synthesis process in VHDL ?

8

UNIT - III

3 (a) Describe the steps of synchronous sequential circuit with suitable example.

8

(b) Explain Moore and Melay machine and describe the clock skew.

8

OR

3 Discuss the concept and working principle of following : (any four)

(i) ROM

(ii) FPGA

(iii) PLA

(iv) PLD

(v) Setup time and Hold time.

16

UNIT - IV

4 (a) What do you mean by event driven circuit ?

8

(b) Explain design procedure of asynchronous circuits.

8

OR

4 (a) What is races and what is process of race free assignment ? 8

(b) Describe all type of Hazard in combination networks. 8

UNIT - V

5 Why we use FPGA kits and explain logic elements and programmability. 16

OR

5 Write short notes on : (any two)

(a) SRAM

(b) Flash Memory

(c) Lookup Table Technology. 16