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4E2086

B. Tech. (Sem. IV) (Back/Old Scheme) Examination, June/July - 2011
Electronics & Comm.
4EI2 Analog Electronics
Common for EC & EIC

Time : 3 Hours]   [Total Marks : 80
                                          [Min. Passing Marks : 24

*Attempt any **five** questions. Selecting **one** question from each unit.*
*All questions are carry **equal** marks.*
Schematic diagrams must be shown wherever necessary. Any data
you feel missing any suitably be assumed and stated clearly).
Units of quantities used/calculated must be stated clearly

Use of following supporting material is permitted during examination.
(Mentioned in form No. 205)

1. _____ **Nil** _____   2. _____ **Nil** _____

UNIT - I

1 (a) Draw the block diagram of a negative feedback amplifier.
        Derive an expression for the voltage gain of an amplifier
        of gain A when subjected to negative feedback with a
        feedback fraction B.

                                                            8

   (b) State the merits and demerits of negative feedback amplifier.
                                                            8

2 (a) Discuss the effect of negative feedback on :
        (i)   Distortion
        (ii)   Output impedance
        (iii) Input impedance

   (b) An amplifier with current feedback has the following
        specifications :

        $h_{fe} = 100\Omega; h_{ie} = 2000\Omega, R_1 = 15000\Omega$

        $R_2 = 5600\Omega, R_e = 100\Omega$ and $R_L = 470\Omega$

        Calculate the values of voltage gain and input resistance of
        the amplifier with and without feedback.

                                                            8

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UNIT - II

3 (a) Find an expression for the frequency of oscillations and condition for sustaining the oscillation in tuned collector oscillator.

8

   (b) Describe Hartley oscillator circuit and explain its action.

8

4 (a) Sketch the circuit of schmitt trigger and explain its operation.

8

   (b) What is a monostable multivibrator ? Explain its working with the help of neat waveform ?

8

UNIT - III

5 Draw the circuit diagram of emitter follower at high frequencies. Also explain its behaviour at high frequencies with necessary expression and parameter.

16

6 Determine gain bandwidth product, unity gain frequency using hybrid π model for CE configuration.

16

UNIT - IV

7 (a) Sketch 2 - input XOR function using static CMOS circuit technique, assume complementary signals are not available.

8

   (b) Explain with neat diagram the working of a totem pole two input TTL NAND gate.

8

8 (a) Explain the parameters used to characterize logic families.

8

(b) Write brief notes on ECL and RTL logic families.

8

UNIT - V

9 (a) Draw the circuit diagram of a push - pull amplifier. Explain its operation. Discuss its advantages and disadvantages.

3+3+2

(b) Show that maximum collector efficiency of class A transformer coupled power amplifier is 50%.

8

10 (a) What do you understand by class A, B and C power amplifiers ?

8

(b) Define and explain the following terms as applied to power amplifiers :
(i) Collector efficiency
(ii) Power dissipiation capability
(iii) Overall gain.

3+3+2